REMARKS

I. Introduction

Claims 1-36 are pending in this application, of which claim 1 is independent. Applicants acknowledge, with appreciation, the Examiner's indication that claims 6-17 and 19-36 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-5 and 8 stand rejected. However, Applicants submit that by the present Remarks, this application is placed in clear condition for immediate allowance.

II. The Rejection of Claims 1-5 and 18

Claims 1-5 and 18 have been rejected under 35 U.S.C. §102(b) as being anticipated by Hamada et al. In the statement of the rejection, the Examiner asserted that Hamada et al. discloses a clock adjusting device which identically corresponds to the claimed subject matter. Specifically, the Examiner asserted as follows (paragraph 6 of the Office Action):

> However, Hamada uses the reference level for detecting the leading and trailing edges of a reference signal (see paragraph 74-88). Applicant argues Hamada does not detect the cross timing, but detecting the edges of a signal is detecting the cross timing of the signal. Hamada uses the reference value to detect the cross timing, calculates a difference between the value of the reproduced data and a zero value at the cross timing, and then updates the reference value, just as required by Applicant's claim language. See the previous rejection.

Applicants respectfully traverse this rejection.

The objective discussed in the present application is to solve the problem of erroneously detecting a zero cross point when a frequency error between the reproduced data and the sampling clock is greater (the section "PROBLEM TO BE SOLVED" on page 4 of the specification and Fig. 27(b)). On the other hand, the objective of Hamada is to obtain a proper amount of phase errors by adjusting a reference level in the phase error detecting part based on

the offset amount of a reproduction signal even if the overall level of the reproduction signal is changed (paragraph [0016]). The objective discussed in the present application is different from that of Hamada et al., which results in differences between the claimed subject matter and Hamada's disclosed circuit, as set forth below.

Applicants submit that Hamada et al. does not disclose, at a minimum, "a phase error calculator for receiving the reproduced data and a cross timing signal from the cross detector and calculating a difference between the value of the reproduced data and a zero value at the cross timing as phase error data," as recited in claim 1.

In the Office Action, the Examiner, referring to paragraph [0093] of Hamada et al., identified offset detecting circuit 68 as the claimed phase error calculator. Paragraph [0093] of Hamada et al. describes, "the offset detecting circuit 68 calculates the offset amount based on the sample value obtained from the trailing edge of said reproduction signal." Applicants believe the that Examiner's position is technologically not accurate because offset detecting circuit 68 detects the offset amount at a trailing edge of the reproduction signal (in other words, not at a leading edge, i.e., a cross point detected by the claimed cross detector, which may correspond to leading edge detecting logic circuit 82 of Fig. 7 of Hamada et al.) (see paragraphs [0093] and [0094], and Fig. 6 of Hamada et al.). Applicants stress that the claimed subject matter does not intend to address such an offset. The claimed phase error calculator is configured for calculating, as phase error data, a difference between (1) a value of the reproduced data at a cross timing detected by the cross detector and (2) a zero value. It is noted that according to Hamada et al., first phase error calculating circuit 61 (see [0056]) may be considered equivalent to the claimed phase error calculator for the sake of this response. In Hamada et al., however, it is the offset amount of the offset detecting circuit (as mentioned above, this circuit is not the phase

error calculator of the claimed subject matter) that updates the reference value, and the output of the first phase error calculating circuit 61, corresponding to the phase error calculator of the present invention, is not at all used for updating the reference value. Therefore, Hamada et al. does not disclose the claimed phase error calculator.

Applicants further submit that Hamada et al. does not disclose, "a cross reference value generator for receiving the phase error data from the phase error calculator and updating the reference value of the cross detector based on the phase error data," recited in claim 1.

Hamada et al. discloses updating a reference value based on the offset amount of offset detecting circuit 68 which is not the claimed phase error calculator. In contrast, the claimed subject matter updates the reference value based on the phase error data from the phase error calculator. In addition, Hamada et al. does not disclose updating a reference based on an output from first phase error calculating circuit 61.

Based on the foregoing, Hamada et al. does not identically disclose a phase error detecting circuit including all the limitations recited in independent claim 1. Dependent claims 2-4 and 18 are also patentably distinguishable over Hamada et al. at least because these claims respectively include all the limitations recited in independent claim 1 Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims and favorable consideration thereof.

III. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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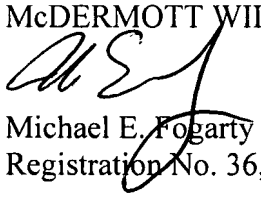

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